Programmable Persistent Interfacial Metallic State Induced by Frozen Ions in Inorganic–Glass Solid Electrolyte

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Electric field control of charge carrier density through dielectric layers has long been a key technology in the semiconductor industry and condensed-matter physics. The new carrier-doping method by the electric double layers (EDLs) opens up the route to access clean carrier doping with high carrier density, but this method is not practical for a switching device due to its slow response to the electric field. However, if this slow response could be stopped at room temperature as an extreme case, the EDL method can become the practical means for materials design, which produces a persistent carrier-doped state without impurity introduction or continuous supply of external electric fields. Here, it is demonstrated that the thermally programmable persistent interfacial metallic state can be realized around room temperature by all-solid heterointerface devices using an inorganic–glass solid electrolyte as a gate insulator. The proposed device, in this study, could pave the way for designing a new category of a highly carrier-doped semiconductor.

1. Introduction

The number of charge carriers is a key parameter to control electronic states of condensed matter systems. As a new control method of charge carrier density, a field-effect transistor (FET) has been intensively investigated due to its controllability of carrier concentration without altering the chemical or structural disorder.[1,2] Recently, a new type of FET, referred to as an electric double-layer transistor (EDLT), is attracting much attention due to its ability to accumulate higher density carriers[3–5] at the interface between a gate insulator and a channel semiconductor, as compared with conventional FETs, gate insulators of which are solid dielectrics.[6–10] In the reported EDLT, an applied gate voltage induces ions transport in a gate insulator, which is an ionic conductor such as a liquid/polymer electrolyte or an ionic liquid, to the boundary between a gate insulator and a semiconductor channel. Charge carriers are accumulated in a semiconductor channel to screen the charge of ions at the interface, and an electric double layer (EDL) is formed, which can be regarded as a nanometer-scale capacitor with high capacity in the range of 1–10 μC cm^{-2}.[11] Since the gate voltage predominantly drops at the interface with EDL, a large electric field of the order of 10 MV cm^{-1}[12] enables the channel to accumulate high-density charge carriers near the interface and to control a wider variety of electronic properties, such as superconductivity,[3,5,13–15] ferromagnetism[16] and metal–insulator transition,[4,17] through electrostatic carrier doping. However, the electronic states induced by FET, including EDLT with gel electrolyte gate,[18] are generally lost when the external electric field is removed around ambient temperature. Although nonvolatile electric-field-induced electronic states are reported in all-solid-FETs with a ferroelectric gate insulator (ferroelectric FETs), the field effect is much smaller than that of EDLT and assisting chemical doping is necessary for electronic phase control.[19,20] Since EDLT is applicable to a wider variety of materials and has the ability to control high density carrier without disorder in bulk, the exploration of a new method to stabilize electric-field-induced states in EDLT as in ferroelectric FET could open a way for tailoring novel interfacial states, such as quasi-2D electron gas found in hetero-interface of two band-insulator oxides.[21,22]

Stimulated by the previous studies, in the present research, we have tried to produce persistent electronic states, which are stable up to around room temperature, in EDLT of $SrTiO_3$ by using an inorganic solid electrolyte as a gate insulator (see **Figure 1**a). Taking advantage of lower mobility of ions in an inorganic solid electrolyte than those in a liquid/polymer electrolyte and ionic liquid, the persistent EDL was formed at the

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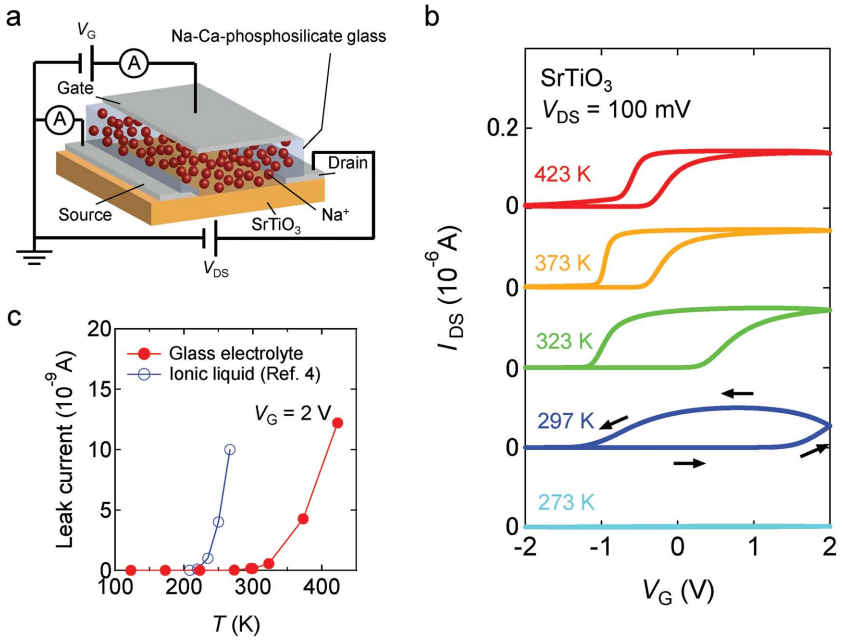

Figure 1. a) A schematic illustration of the EDLT with inorganic solid electrolyte, Na–Ca–phosphosilicate glass, as a gate insulator. Only mobile cations, Na^+ ions, are shown with red spheres in the gate insulator of Na–Ca–phosphosilicate glass. b) Transfer characteristics of EDLT with a gate insulator of solid electrolyte, Na–Ca–phosphosilicate glass, on the $SrTiO_3$ channel. During measurements, a drain-source voltage, V_{DS}, was kept at 100 mV. The gate voltage, V_G, was swept from −2 to 0, then to +2 V, and finally back to −2 V. The sweeping process of V_G is shown by arrows for 297 K. The gate leak current was negligibly small compared with the drain-source current, I_{DS}. The curves are shifted vertically for clarity. c) Temperature dependence of the leak current of EDLT with a gate insulator of inorganic–glass electrolyte between gate and source electrodes at V_G = 2 V (closed red circles). The leak current of EDLT with an ionic liquid is shown for comparison by open blue circles.[4]

interface between the solid electrolyte and $SrTiO_3$ by freezing the motion of ions in the gate insulator of EDLT. Here, we report the programmable persistent interfacial metallic state realized by producing persistent EDL through the thermal poling process, in which the sample is cooled down under the applied voltage.[23]

2. Results and Discussion

2.1. FET-Performance Dominated by Mobile Cations in Gate Insulator of Inorganic–Glass Solid Electrolyte

As a gate insulator of EDLT for $SrTiO_3$, Na–Ca–phosphosilicate glass was chosen. The homogeneous thin film of glass was successfully prepared by pulsed laser deposition (PLD) (see Figure S1 in the Supporting Information). The oxygen pressure in the deposition chamber was kept at ≈1×10^{-4} Torr during the film growth to suppress production of oxygen vacancies (see Figure S2 in the Supporting Information). The insulating state of $SrTiO_3$ was checked to be remained even after thin film growth, which indicates the formation of a metallic layer by a chemical reaction was suppressed as reported in other FETs prepared by PLD.[24] Na–Ca–phosphosilicate glasses are known as inorganic solid electrolytes, in which only Na^+ ions are mobile.[23,25,26] In recent theories, it has been suggested that the mobile ions in a solid electrolyte, which can directly adsorb on the interface, could give a larger interfacial capacitance than that predicted from a mean field theory,[27,28] which assumes the averaged dielectric constant of a solid electrolyte. Taking into account the fact that the large interfacial capacitance over 100 μC cm^{-2} is observed in the AC-impedance measurements for Na–Ca–phosphosilicate glasses (Figure S3, Supporting Information) as reported in the previous study,[25,26] the effective accumulation of a charge carrier could be expected at the Na–Ca–phosphosilicate glasses/$SrTiO_3$ interface in EDLT. A $SrTiO_3$–EDLT gated with Na–Ca–phosphosilicate glass showed an n-type transistor operation above room temperature. Figure 1b displays the gate-voltage (V_G) dependence of drain-to-source current (I_{DS}) at varied temperatures. As shown in Figure 1b, the drain-source current (I_{DS}) increases with scanning of the gate-voltage (V_G) in the positive direction in the low voltage range between −2 V and 2 V. The n-type FET behavior is consistent with the previous reports of the FET with $SrTiO_3$, in which oxides,[6,7] organic polymer,[9] and electrolyte [3,29] are used as gate insulators.

As shown in Figure 1b, one can see the anticlockwise large hysteresis loops in the V_G versus I_{DS} curves, the width of which becomes narrower as the temperature increases. Since the origin of hysteresis loops could be ascribed to the delay of cations motion to the change of V_G, the narrowing hysteresis indicates that the response time of cations to the sweeping V_G becomes fast in the glass electrolyte as temperature increases. At room temperature, 297 K, reflecting slow cations motion, the I_{DS} saturates after switching the sign of sweeping direction of V_G from positive to negative. On the other hand, above room temperature with high mobility cations, the I_{DS} almost saturates in the V_G scan for the positive direction. The on-off ratios above room temperature were ≈10^2. Below room temperature, the current enhancement by electrostatic gating voltage was hardly observed, indicating that the motion of cations in a glass electrolyte was frozen.

Ionic conductivity by mobile cations in a gate electrolyte contributes to the leak current of EDLT.[4] As shown in Figure 1c, the leak current of EDLT with a gate insulator of inorganic–glass electrolyte is a negligible value smaller than 10^{-11} A below room temperature, indicating remarkable decrease in ionic conductivity due to freezing of ions motion. The temperature dependence of leak current is consistent with that the hysteresis is remarkably suppressed in the I_{DS}–V_G measurements below room temperature (Figure S4, Supporting Information). Reflecting low ionic mobility of solid electrolyte, the freezing temperature of mobile ions in the inorganic–glass is higher than that of the ionic liquid,[4] ≈210 K, as compared in Figure 1c.

Below the freezing temperature of cations in the inorganic–glass electrolyte, the interface with EDL could be maintained as

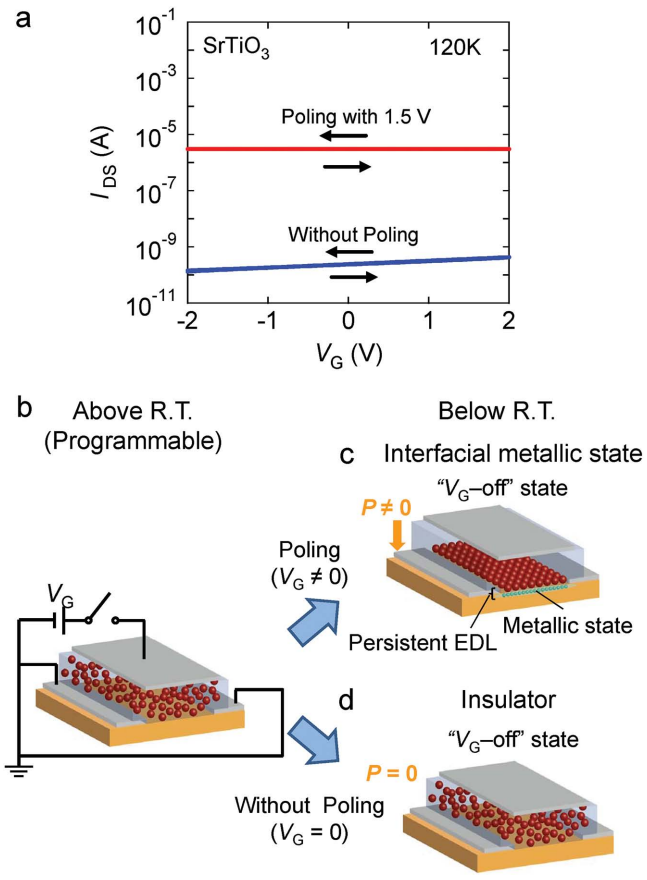

Figure 2. a) Transfer characteristics measured at 120 K under the different cooling conditions. The curves with higher I_{DS} (red curve) and lower I_{DS} (blue curve) were obtained after cooling with poling and without poling process, respectively. In the poling process, the sample was cooled down to 120 K while applying voltage of +1.5 V to gate electrode. This poling voltage was turned off before the measurement of V_G–I_{DS} curves. In the measurement of transfer characteristic, the gate voltage, V_G, was swept from −2 to 0, then to +2 V, then to 0 V, and finally back to −2 V. b) A schematic drawing of circuit above room temperature. The electronic state becomes programmable by gate voltage because ions in a solid electrolyte are movable. c) A schematic drawing of persistent EDL produced by freezing ions motion in inorganic–glass solid electrolyte (thermal poling procedure). After cooling the sample with applying V_G, the gate voltage is turned off. At enough low temperature for ions motion to freeze, the electric polarization, P, in a glass electrolyte is maintained without V_G and electron carriers are accumulated to screen the interface charge in the semiconducting channel, forming EDL. Persistent metallic state induced at the interface between Na–Ca–phosphosilicate glass and $SrTiO_3$ by EDLT is schematically displayed. d) A schematic drawing of a glass electrolyte/$SrTiO_3$ EDLT cooled without gate voltage. In this freezing state, Na^+ ions do not response to V_G—sweep and charge accumulation does not occur.

a persistent state even if a voltage is removed. In **Figure 2**a, the V_G–I_{DS} curve measured at 120 K after a thermal poling process (Figure 2b,c), in which the sample is cooled down from above room temperature while applying voltage to the gate electrode, is compared with that without the poling process (Figure 2b,d). In both the curves, the drain-source currents show almost independent behavior to V_G, reflecting that ions motion is frozen in the inorganic–glass electrolyte. In the case of cooling down to 120 K from above room temperature with a poling voltage, +1.5 V, the I_{DS} was four orders of magnitude larger than that without the thermal poling process due to the formation of persistent EDL at the interface between the inorganic–glass solid electrolyte and $SrTiO_3$ with carrier accumulation, as schematically shown in Figure 2c. When the sample was cooled down without a poling voltage, the I_{DS} showed only a small value below 1 nA because no EDL was formed, resulting in no carrier accumulation, as schematically displayed in Figure 2d. The recovery to its initial state by melting frozen ions was confirmed after the poling procedures (Figures S5 and S6, Supporting Information). These results indicate that the persistent electronic state can be thermally programmable at above room temperature.

2.2. Persistent Interfacial Metallic State Produced by the Frozen Ions at the Interface between Inorganic–Glass Solid Electrolyte and $SrTiO_3$

Figure 3a,b displays the temperature dependence of sheet resistance, R_{sheet}, and sheet carrier density, $-1/R_H e$, respectively. They were measured without applying a gate voltage after thermal poling. As shown in Figure 3a, metallic behavior is observed up to around room temperature in the channel of $SrTiO_3$, the nondoped bulk of which is insulating, even after the gate voltage is turned off. This result indicates that persistent electronic state is realized. The metallic state after the poling process was nonvolatile for periods of hours (the length of the experiments). When the sample was heated above room temperature in vacuum, the recovery of insulating state of $SrTiO_3$ was confirmed (see Figure S6 in the Supporting Information), indicating that the nonvolatile metallic state is not due to the formation of irreversible chemical reaction layers. In the case that a large electric field of the order of 10 MV cm^{-1}[12] is applied to the interface of transition metal oxides and ionic liquid by EDL, the effect of oxygen vacancy formation to conductivity has been proposed[30,31] and still is a matter of controversy at present.[32] Taking into account that the metallic state induced by oxygen vacancy is irreversible,[30] the electrostatic effect seems to be more dominant than that of oxygen vacancy in our results because the recovery to the initial insulating state was observed above room temperature in vacuum after the thermal poling measurements (Figures S5 and S6, Supporting Information). The identification of origin for a nonvolatile metallic state is a quite interesting matter, but unfortunately it is beyond our current facilities. A further study by secondary mass spectroscopy using an oxygen isotope could make clear the contribution of oxygen vacancy to the electronic conductivity in the future work.

The sheet resistance of metallic state is below the quantum resistance $h/e^2 \approx 25.8$ kΩ for 2D systems. The Hall coefficient, R_H, is found to be negative as shown in Figure 3b, which is in agreement with accumulation of electron carriers by positive poling voltage. As displayed in Figure 3b, the sheet carrier density of metallic state is about 1×10^{14} cm^{-2}, which is the same order of sheet carrier density reported in the systems with 2D superconductivity as a ground state.[3,33] Taking into account that the sheet resistance below ≈200 K is under the quantum

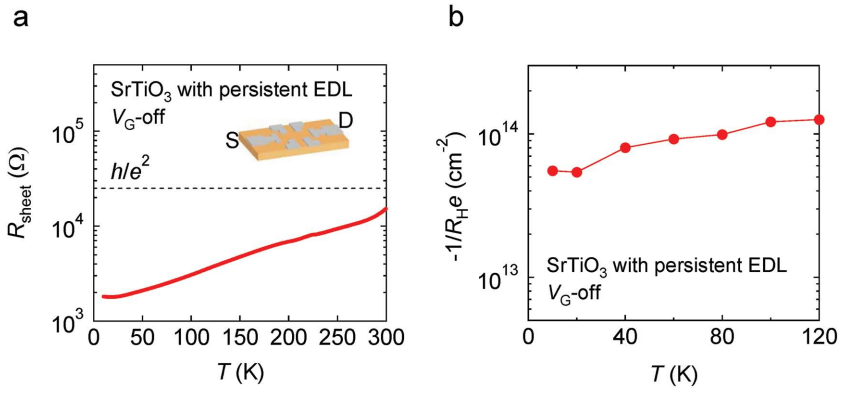

Figure 3. Transport properties measured after poling procedures. In the poling procedures, the sample was cooled down to 10 K from above 300 K while applying voltage of +3.0 V to the gate electrode. This poling voltage was removed before the measurement of R_{sheet} and Hall effect. a) Temperature dependence of sheet resistance, R_{sheet}, after poling procedure. R_{sheet} was measured without applying gate voltage (V_G-off). The inset shows the Hall bar configuration of electrodes for measurements of R_{sheet} and Hall coefficient, R_H. b) Temperature dependence of sheet carrier density, $-1/R_He$, obtained from Hall effect measurement after the poling procedure. The Hall effect was measured without gate voltage (V_G-off).

critical resistance for pairs, $h/(2e)^2 \approx 6.45$ kΩ, a 2D superconducting state might be expected as a ground state of the persistent metallic channel of $SrTiO_3$ at enough low temperature below 1 K.[3,33–36]

To confirm dimensionality of the persistent electronic state induced by the frozen cations in the inorganic–glass electrolyte, we measured anisotropy of transverse magneto resistance (MR). **Figure 4**a shows the change ratio of sheet resistance, $\Delta R_{sheet}(\mu_0 H)/R_{sheet}(0)$, in the magnetic field (H) perpendicular to the plane and parallel to the plane (see Figure 4b). Here, $\Delta R_{sheet}(\mu_0 H)$ is the change of sheet resistance in magnetic fields and $R_{sheet}(0)$ is the zero-field resistance at 10 K. The clear positive MR is observed only for the H perpendicular to the plane. Taking into account that the crystal structure of $SrTiO_3$ is pseudo-cubic,[37] anisotropic MR might be attributed to the anisotropy of electronic state as one possible scenario. In this case, suppression of MR for the H parallel to the plane indicates that the thickness of metallic layer is thinner than the cyclotron radius of electrons. However, since the partially filled interfacial sub-bands of $SrTiO_3$ can induce ferromagnetism, anisotropy of magnetism might be also included in the anisotropic MR.[38] Magnetic field dependence of quantum conductance oscillations could be a convincing way to determine the dimensionality of persistent metallic states.

So far, persistent 2D electron gases have been mainly investigated through accumulation of charge carrier at the hetero-interfaces between two thin films of distinct insulators fabricated by the epitaxial method and in the amorphous hetero-structures.[20,21,39–42] The 2D electron gas found at the interface between two band insulators has triggered an intense research effort and leads to discovery of the fascinating characteristics, such as 2D superconductivity,[33] magnetism at the interface,[43] and giant thermoelectric power.[44] However, for hetero-interfaces prepared by the epitaxial method,[20,21,40–44] available materials are limited due to matching condition of lattice constants of two insulators. The new method suggested in this study, in which EDL is stabilized by ion freezing in polarized inorganic glass electrolyte, might enlarge the possibilities of applications for a wide variety of materials, because matching of lattice constants is unnecessary for the interface between semiconductor and amorphous inorganic–glass. Furthermore, since space inversion symmetry is inherently broken at any interface, persistent quasi-2D electron gas, which might be induced at the interface between inorganic–glass electrolyte and semiconductor including atoms with large atomic number, could be a novel platform to investigate the effect of spin–orbit interaction, such as the Rashba effect.[45]

3. Conclusion

In summary, we have demonstrated that freezing motion of cations in polarized inorganic–glass solid electrolyte can induce a persistent interfacial metallic state as a thermally programmable electronic state at the interface between the inorganic–glass solid electrolyte and $SrTiO_3$. Above room temperature, a performance as an n-type transistor, which accompanies hysteresis loops reflecting delay of cations motion to sweeping gate voltage, was observed for low $|V_G|$ smaller than 2 V. Cooling the sample below room temperature, at which the motion of Na^+

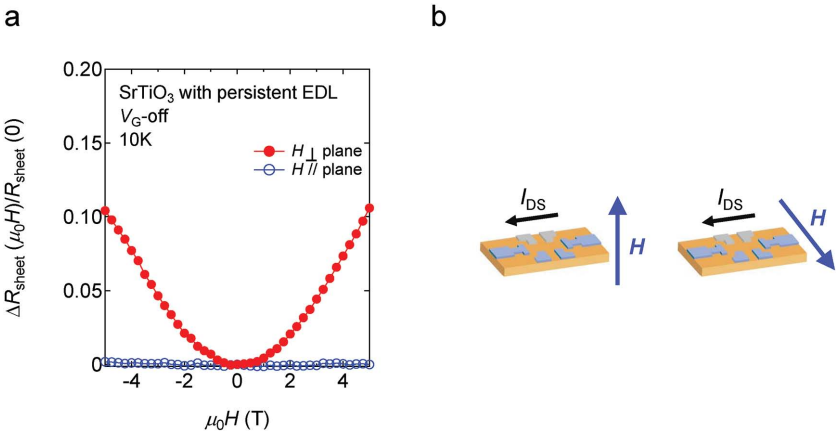

Figure 4. Anisotropic magneto-resistance measured after poling procedures. a) Transverse magnetoresistance (MR) $\Delta R_{sheet}(\mu_0 H)/R_{sheet}(0)$ measured in the two different directions of magnetic fields at 10 K. Closed red circle and open blue circle represent the MR obtained in the perpendicular and the parallel fields to the glass electrolyte/$SrTiO_3$ interface, respectively. b) The directions of magnetic fields to the interface are schematically displayed for perpendicular and parallel configurations. The shaded (blue) electrodes are used for MR measurements.

ions is frozen, with applied poling voltage, the metallic interface in the $SrTiO_3$ channel was stabilized. The induced metallic state was maintained up to around room temperature even when the gate voltage was removed. We confirmed the quasi-2D anisotropy and carrier density of the order of 1×10^{-14} cm^{-2} in the induced metallic state through magnetoresistance measurements. EDLT with an inorganic–glass solid electrolyte as suggested in this study would enable us to make all-solid-device with high density integration. The stabilization method of EDL by freezing ions may open new routes to design persistent carrier-doped interfacial states freed from disorder around room temperature, in which carrier-doping level is programmable by the thermal poling procedure, and give a platform for novel interfacial phases in a wide variety of semiconductors.

4. Experimental Section

Thin Film Growth of Inorganic-Glass Electrolyte for a Gate Insulator in FET: To employ Na–Ca–phosphosilicate glass as a gate insulator, preparing homogeneous thin films by pulsed laser deposition (PLD) was tried. The films were prepared at room temperature with a 99.9% glass ceramic target (20 mmϕ, TOSHIMA), the composition (mol%) of which is 44.6 SiO_2–31.2 Na_2O–23.2 CaO–1.0 P_2O_5.[25] During the growth of films, the oxygen pressure in the deposition chamber was kept at $\approx 1 \times 10^{-4}$ Torr to obtain insulating $SrTiO_3$ by suppressing production of oxygen vacancies (Figure S2, Supporting Information). The surface of Na–Ca–phosphosilicate glass films synthesized by PLD was observed by using a scanning electron microscope (SEM). Figure S1a and S1b (Supporting Information) shows the surface morphologies for thin films of Na–Ca–phosphosilicate glass grown by using the excimer lasers with different wave lengths, KrF (248 nm, 5.0 eV) and ArF (193 nm, 6.4 eV), respectively. The surface morphologies of thin films show clear dependence on the laser wave length. Although the thin film grown by the KrF excimer laser shows the inhomogeneous morphology including droplets within film as shown in Figure S1a (Supporting Information), the homogeneous thin film was obtained successfully by using the ArF excimer laser with higher photon energy than the KrF laser as displayed in Figure S1b (Supporting Information). The difference of thin film quality, which depends on the laser energy, could be attributed to the different optical absorption at each photon energy in Na–Ca–phosphosilicate glass, as reported in other amorphous glasses with wide energy gap.[46] If the photon energy is not large enough to the energy gap of glass, which is about 5 eV as shown in Figure S1c (Supporting Information), optical absorption is suppressed and incident light penetrates deeply into the target of bulk glass. The penetrated light would be absorbed by defects inside the bulk, and the target material might be ejected to the substrate as droplet forms, which is observed in the thin film grown by using the KrF excimer laser (see Figure S1a in the Supporting Information). On the other hand, when the photon energy is large enough for light to be absorbed, the surface layer is efficiently ablated as a vapor phase and homogeneous thin films could be grown on the substrate as shown in Figure S1b (Supporting Information). In this study, the ArF excimer laser (Coherent COMPexPro 102) was used for the preparation of glass electrolyte film as a gate insulator in FET structure.

Fabrication of the FET-Structure with a Gate Insulator of Inorganic Solid Electrolyte, Na–Ca–Phosphosilicate Glass: Since electrochemical active ions such as H^+ or OH^-, which would originate from H_2O contained in gate insulators, are known to cause chemical reaction such as water electrolysis at the interface between the electrolyte and the semiconductor channel,[47,48] we fabricated the FET structure by a dry process. The FET structures (Figure 1a) were fabricated on the (001)-face of $SrTiO_3$ single-crystal substrates (10 mm × 10 mm × 0.5 mm, SHINKOSHA). Six electrodes (Al (or Ag) electrodes with thickness of 30 nm, channel size: 400×600 μm^2) in a Hall-bar configuration were first evaporated using a stainless shadow mask (see the inset of Figure 3a). Then, Na–Ca–phosphosilicate glass films of ≈250 nm thickness were prepared by pulsed laser deposition (PLD). After the growth of Na–Ca–phosphosilicate glass film as a gate insulator, a 30 nm thick metallic Al (or Ag) electrode was evaporated as a gate electrode through a stainless shadow mask. In the case of measurement of sheet resistance or Hall effect, an Au wire was attached by a conducting Ag paste. The insulating behavior of the FET was checked to confirm that the nonvolatile metallic state was not formed as a reaction layer in the FET-fabrication process.

Electronic Transport Properties: The transport characteristics of the FETs were measured by the DC two-probe method with a semiconductor parameter analyzer (Agilent B1500A) connected to a vacuum probe station (Riko-boeki). The measurements were performed in a vacuum of $\approx 1 \times 10^{-6}$ Torr to suppress oxidization of the devices. A drain-source voltage (V_{DS}) was kept at 100 mV during sweeping gate voltage (V_G), the sweep speed of which was 37 mV s^{-1}, between −2 V and 2 V. The transfer characteristics of FET below room temperature are displayed in Figure S4 (Supporting Information). The measurements of sheet resistance and Hall effect were carried out by the DC four-probe method. They were performed by a combination with a physical property measurement system (PPMS, quantum design) and two DC voltage/a current sources to control of V_G (Yokogawa 7651) and V_{DS} (ADCMT 6144), and picoammeter (KEITHLEY 6485) to monitor the drain-source current (I_{DS}). Before the measurements of sheet resistance and Hall effect, gate voltage, V_G = +3 V, was applied above 300 K for about 1 h until the I_{DS} was saturated. Then, the device was cooled down to 10 K and the applied gate voltage was turned off. The sheet resistance and Hall coefficient were measured without applying V_G. The measurement of Hall effect and transverse magneto-resistance were performed by applying a magnetic field perpendicular to the I_{DS} between −5 T and 5 T.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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